Novel Direct-Coupled Current Switch Architecture for a Series-Connected Voltage-Balancing Pulse Driver

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Abstract — **A series-connected voltage-balancing circuit can output n-times larger voltage swing than can be output by a single transistor, where n is the number of series-connected transistors. This circuit makes it possible for high-speed low-breakdown-voltage transistors to be applied to large-voltage-swing pulse drivers, such as an optical modulator driver. This paper reports the first operation of this type of driver at 10 Gbit/s. Novel direct-coupled current switch architecture prevents FETs exceeding gate-drain breakdown voltage and keeps high-speed operation. The fabricated driver demonstrated 3.7 V_{pp} (7.4 $V_{pp,\ diff}$) output with clear eye opening.**

I. Introduction

The optical modulator driver is a key component for high-speed fiber-optic communications systems. Though faster transistors are required for faster operation of the driver, the breakdown voltage generally decreases as the transistor speed increases. This makes it difficult to develop a high-speed large-voltage-swing driver circuit.

One solution to this problem is to employ a distributed-amplifier configuration combined with rather-low-speed high-breakdown-voltage transistors [1], [2]. Nevertheless, the transistors used in these ICs cannot be applied to digital circuits at the same bit rate as the ICs operate because of the shortage of device speed. In addition, the group delay characteristics of the distributed amplifier degrade at frequencies considerably lower than the cutoff frequency of the amplifier.

To integrate digital functional blocks with high-output-voltage drivers, circuit technology that enables large output voltage swing using high-speed transistors with rather low breakdown voltage is required. For this purpose, series-connected voltage-balancing circuit configuration is promising. This configuration has been developed and been used in power electronics for low-speed high-voltage switching [3]-[5] where the difficulty is in keeping voltage balance during switching. If the voltage balance breaks, one transistor may exceed the breakdown voltage and burn out. Therefore, many practical high-voltage switches employ protection devices, such as Zenor diodes, in parallel to the transistors [5]; however, these devices decrease the operating speed and, accordingly, cannot be adopted in high-speed pulse driver circuits. In addition, delay between sequential switching of series-connected transistors might distort the eye-pattern when the circuit is applied to signal transmission. Thus, this type of circuit has not been applied to high-speed signal transmission circuits, such as optical modulator drivers until recently. In 1997, the first trial for a modulator driver was done by T. K. Woodward, et al. [6], which used series connected CMOS. However, the maximum operating speed remained only 155 Mbit/s due to the limitations of the circuit configuration and device speed. By employing current switch configuration, such as source-coupled FET logic (SCFL), high-speed operation will be possible because the transistor can operate in the saturation region of the transistor I-V curves. The operating speed can be boosted by using high-speed transistors with rather low breakdown voltages.

This paper presents a series-connected voltage-balancing pulse driver in novel direct-coupled current switch architecture. The architecture solves the problem of voltage balancing between series-connected FETs during switching. By employing high-speed SCFL circuits and high-speed but rather low-breakdown-voltage transistors, high-speed operation of the driver is achieved. A data transmission experiment demonstrates that this type of driver can transmit signals with sufficiently good waveform qualities.

II. Design

Figure 1 illustrates the principle of voltage-balancing operation of series-connected FETs when two FETs are used for the balancing. The key point is that during the operation the gate-source voltages (V_{gs}) of the two FETs (lower: T_1, upper: T_2) are applied equally so as to keep the drain-source voltage (V_{ds}) of the two FETs equal. This operation divides the voltage applied between the

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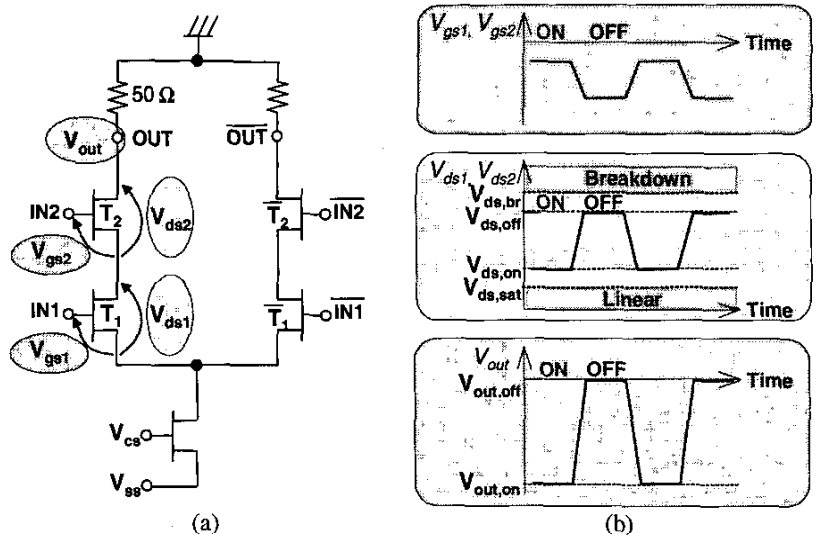

Fig. 1. Principle of voltage-balancing operation by series-connected FETs (T_1, T_2) when two FETs are used for the balancing. (a) Series-connected current switch. (b) Illustrated time transition of gate-source voltage (V_{gs1}, V_{gs2}), drain-source voltage (V_{ds1}, V_{ds2}), and output voltage (V_{out}) when the left side of the current switch is on and off.

source of T_1 and the drain of T_2 equally. Consequently, the output voltage (V_{out}) swing is the sum of the change of the V_{ds}'s of T_1 and T_2, and it can be twice as much as the swing that can be output by a single FET.

Though the concept of the series-connected voltage-balancing operation is simple, the difficulty lies in the control sequence of series-connected FETs. That is, if the control timing between gate and source of the upper FET differs during switching, the FET tends to suffer exceeding the breakdown voltage and will be damaged.

Figure 2 shows how the waveform of V_{gs}, V_{ds} and the gate-drain voltage (V_{gd}) of the upper series-connected transistor, T_2, (V_{gs2}, V_{ds2} and V_{gd2}) differs when the control timing of the gate and source voltage of the same FET (V_{g2} and V_{s2}) changes. Figures 2(a) and (b) are the waveforms when V_{in1} and V_{in2} (i.e. V_{g2}) are controlled simultaneously. Large undershoots in V_{gs2}, V_{ds2} and V_{gd2} are observed at the beginning of the transition at a time of around 100 ps, which corresponds from ON to OFF for T_2, and at the beginning of the transition at a time of around 200 ps, which corresponds from OFF to ON for T_2. The undershoot in V_{gd2} is especially serious because the voltage breakdown of an FET is limited in V_{gd} for normal compound semiconductor FETs. These undershoots are caused by the control timing difference between V_{g2} and V_{s2}. Due to the delay from the input of T_1 (IN1) to the source of T_2, the control timing of V_{g2} is approximately 6-ps earlier than that of V_{s2} when V_{in1} and V_{in2} are controlled simultaneously.

This problem can be solved by adding an appropriate delay to the control timing at IN2 so as to synchronize the control timing of V_{g2} and V_{s2}. By adding 6-ps delay to the control timing at IN2, the undershoots for the transition at a time of around 100 ps and 200 ps are much reduced as shown in Fig. 2(c) and (d). The undershoot in V_{ds2} still remains to some extent because it is inherent for this type of sequential switching from T_1 to T_2. This inherent undershoot originates from the delay between the switching of T_1 and T_2, which breaks the voltage balance in V_{ds} during the time that T_1 becomes ON and T_2 is still OFF. Nevertheless, this is not serious because the maximum output voltage swing is limited not by V_{ds} but V_{gd}. Fortunately, the remained undershoot in V_{gd2} is slight after the control-timing synchronization between V_{g2} and V_{d2}.

To include the control-timing synchronization in the design of series-connected voltage-balancing driver circuit, we employed novel direct-coupled current switch architecture as shown in Fig. 3. In this architecture, the gate of T_1 is controlled directly from the input signal at terminal IN, while the gate of T_2 is controlled through the current switch without a source-follower circuit. In this architecture, the delay from terminal IN to the gate of T_2 (path A) is designed to be approximately the same as the delay from terminal IN to the source of T_2 (path B) to suppress undershoots in V_{gd} for T_2.

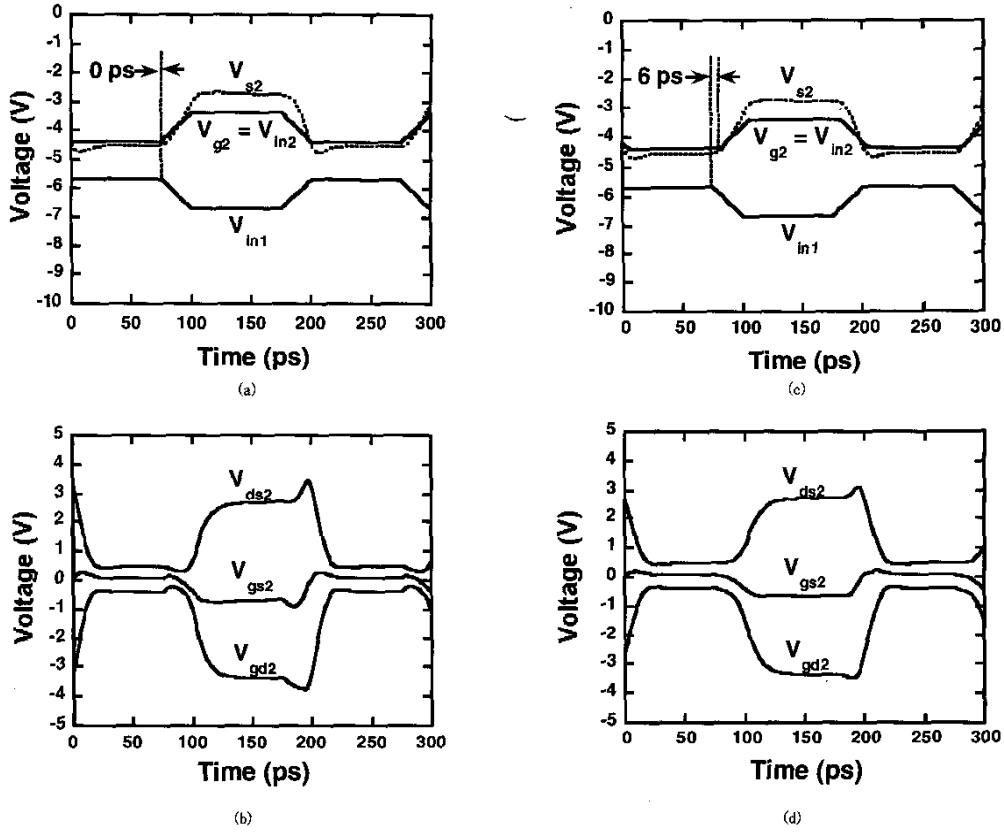

Fig. 2. Impact of control timing between IN1 and IN2 on V_{gs2}, V_{ds2} and V_{gd2} of upper series-connected FET (T_2) by circuit simulation. (a) Waveforms at IN1 (V_{in1}), IN2 (V_{in2}), and source voltage (V_{s2}) of T_2 when V_{in1} and V_{in2} are controlled simultaneously. (b) Waveforms of V_{gs2}, V_{ds2} and V_{gd2} of T_2 when the input voltages are as shown in (a). (c) V_{in1}, V_{in2} and V_{s2} of T_2 when V_{in2} is delayed for 6 ps form V_{in1}. (d) V_{gs2}, V_{ds2} and V_{gd2} of T_2 when the input voltages are as shown in (c).

III. Expeiment

The driver circuit shown in Fig. 3 was fabricated using 0.1-μm InP HEMT process [7] with a g_m of 1.05 S/mm, a V_t of -0.53 V, and an f_T of 165 GHz. In the design, the V_{ds} at the off-state is set to 2.7 V so as not to exceed a tentative V_{gd} limit for the design of -4 V. By setting V_{ds} at the on-state to 0.55 V, the output voltage swing of single FET is 2.15 V_{pp}. Because the voltage swing decrease due to the level shift diode is 0.3 V_{pp}, the designed output voltage swing of the driver is 4 V_{pp}. A gate width of 200 μm is used for the FETs.

Figure 4 shows a photomicrograph of the fabricated driver chip. The chip size is 1.12 x 1.84 mm. Power supply voltages for V_{ss}, V_{cs} and V_{dd} are respectively -7.3 V, -7.3 V and -3.4 V and the power dissipation is 0.96 W.

The signal transmission experiment was performed on wafer using an Anritsu MP1761B 12.5-Gbit/s pulse pattern generator and a Hewlett-Packard HP54750A digitizing oscilloscope mainframe with an HP54752A 50-GHz module. Figure 5 shows the output waveforms for the input of 10-Gbit/s pseudorandom bit stream (PN 2^{31}-1). A clear eye opening was observed. This result proves that the degradation in transmission quality by nonlinear operation due to sequential switching of series-connected FETs is sufficiently allowable for 10-Gbit/s NRZ data.

IV. Conclusion

Novel architecture using direct-coupled current switches for a series-connected voltage-balancing pulse driver is described. This architecture synchronizes the

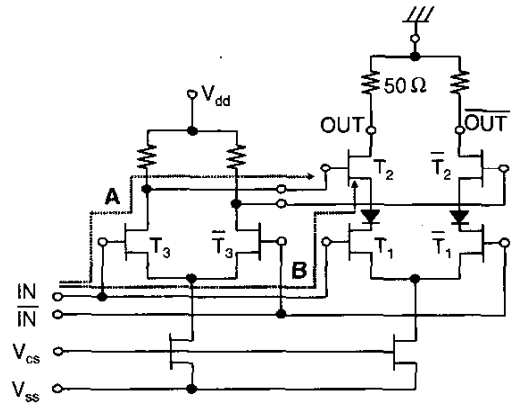

Fig. 3. Circuit diagram of series-connected voltage-balancing pulse driver in novel direct-coupled current switch architecture. The delays though path A and path B are approximately the same.

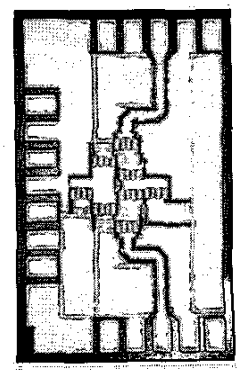

Fig. 4. Photomicrograph of fabricated driver IC. Chip size is 1.12 x 1.84 mm.

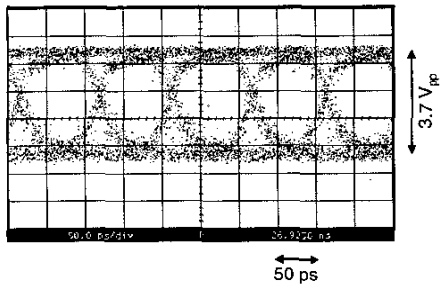

Fig. 5. 10-Gbit/s output waveform of the driver. The input signal is 10-Gbit PN 2^{31}-1 pseudorandom bit stream.

gate and source control timing of the upper FET of series-connected FETs. This suppresses the undershoot in V_{gd} that occurs when the gates of both series-connected FETs are controlled simultaneously and consequently prevents exceeding the gate-drain breakdown voltage. This results in a substantial increase of output voltage swing by decreasing the surplus margin for V_{gd}. An on-wafer measurement experiment showed that the fabricated driver IC has 3.7 V_{pp} single output and 7.4 $V_{pp,diff}$ differential output with clear eye opening for 10-Gbit/s PN 2^{31}-1 data patterns. The driver also demonstrated that the series-connected voltage-balancing circuit in the direct-coupled current switch architecture can be applied to the optical modulator driver for high-speed fiber-optic communications systems.

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